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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/841,875	04/26/2001	Kyung Y. Cho	1465.01	6123

29338 7590 04/02/2004

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EXAMINER	
PAN, DANIEL H	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 04/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/841,875	CHO ET AL.	
	Examin r	Art Unit	
	pan	2183	

-- The MAILING DATE f this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1,3-10,12-16,18,20-27 and 29-32* is/are rejected.

7)☒ Claim(s) *2,11,17,19,28 and 33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *26 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/26/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1,3-10,12-16,18,20 –27,29-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tessarolo et al. (6,567,910) in view of Shinagawa (5,126,541) .

2. As to claim 1, Tessarolo disclosed a system including at least :

a) a) universal register files for storing data and address (e.g. se);

b) program pointer [PC] for storing program addresses (col.6, lines 59-61),;

c) status register for indicating the status of the CPU and a break register (see the status register and the break register [DBGM] register in fig.15);

d) data communication unit for performing data communication with a host (see the interface with the debug host in col.5, lines 21-29);

e) a status register having a flag for representing whether the CPU was in operational mode or a debugging mode (see the status register and the break register [DBGM] register in fig.15);

f) debugging stack pointer [SP] which was used as a stack pointer for pointing to a stack memory (see stack memory in col.6, lines 64-67, col.7, lines 1-1-3).

3. Tessarolo did not specifically show the conversion into the debug mode if a comparator for comparing the value stored in the break register with a break data was

the same as claimed. Tessarolo showed the conversion into the debug mode (see col.5, lines 37-40, col.18, lines 46-56). Tessarolo also showed the debug break register [DBGM] was a mask bit (e.g. col.18, line 34), but no comparator or circuit for comparison to the break mask bit was shown. However, Shinagawa dislocated a system comprising a comparator circuit for comparing a value with a break value [stop register] (e.g. see the comparison of the memory address with the value of stop register in col.6, lines 31-68, col.7, lines 1-2). It would have been obvious to one of ordinary skill in the art o use the Shinagawa for converting into the debug mode based on the result of the comparator as claimed because the use of Shinagawa could provide Tessarolo the integrated capability of the debug mode with the comparison result at a specific break point, therefore providing the flexible connectivity with a specific CPU core without additional circuit overheads, and it could be readily achieved by defining the comparator of Shinagawa into the configuration file of Tessarolo so that the read/write ports of the comparator of Shinagawa could be recognized by Tessarolo, and because Tessarolo did disclose that his break register was a mask (col.18, line 34), which was recognizable by one of ordinary skill in the art that the applicability of the comparison of the break value was possible due to the maskable nature of the break register content, and for the above reasons, provided a motivation.

4. AS to claims 3,20, Tessarolo also included program counter (e.g. see col.6, lines 49-68).

5. As to claims 4,6,10,21,23, 27, Tessarolo's break register [fig.15 [DBGM] was also a mask register (e.g. see the mask bit in col.18, lines 34-35).

6. As to claims 5,22, Tessarolo's break data was also a memory address (e.g. see the break point of particular data location in col.5, lines 21-39).

7. As to claims 7-9, 24-26, Tessarolo also included input and output from the CPU (see the read and write data bus of the CPU in col.7, lines 31-45).

8. AS to claim 12,29, Tessarolo also included separate data and program memory storages (see the separated data space and program memory space in fig.2, and col..6, lines 7-30).

9. As to claims 13,30, Tessarolo also included separated debug and general program memory (see the set aside vector memory in col.6, lines 31-32, see how the debug enabled the interrupt vectors in col.23, lines 25-33).

10. As to claims 14,31, Shinagawa also included downloading of application program (e.g. see col.2, lines 42-47).

11. As to claim 15, Tessarolo's status value was also stored into the memory [the stack memory] designated by stack pointer [SP] (e.g. see the value saved on the stack in col.18, lines 40-55).

12. As to claims 16, 32, Tessarolo also included temporary storage (e.g. see col.26, lines 9-14).

13. Claims 2, 19 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record teaches the combined features of the reset data storage and reset comparator.

14. Claim 11, 28 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record teaches the loading of the different debugging addresses according to the select signal when the break value is the same.

15. Claim 17 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

16. Claim 33 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the combined features of the reference data , the reference comparator, and the loading of the start address if the data input is the same as the reference data.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Goto et al. (6,223,275) is cited for the background teaching of the break point register (e.g see col.4, lines 22-36, col.6, lines 45-64).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).